AMENDMENTS TO THE CLAIMS:

Please amend claim 1 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A data processing apparatus, comprising:

a processor core for executing instructions from any of a plurality of instruction sets;

a prefetch unit for prefetching instructions from a memory prior to sending those instructions to the processor core for execution;

prediction logic for predicting which instructions should be prefetched by the prefetch unit, the prediction logic ~~being arranged to review~~for reviewing a prefetched instruction to predict whether execution of that prefetched instruction will cause a change in instruction flow, and, if so, ~~to indicate~~for indicating to the prefetch unit an address within said memory from which a next instruction should be retrieved;

the prediction logic further ~~being arranged to predict~~for predicting whether the prefetched instruction will additionally cause a change in instruction set, and, if so, ~~to cause~~ for causing an instruction set identification signal to be generated for sending to the processor core to indicate the instruction set to which said next instruction belongs.

2. (original) A data processing apparatus as claimed in Claim 1, wherein the prediction logic is arranged to detect the presence of an instruction of a first type which when executed will cause a change in instruction set if execution also results in said change in instruction flow.

3. (original) A data processing apparatus as claimed in Claim 2, wherein execution of said instruction of the first type will unconditionally cause said change in instruction flow, and wherein the address within said memory from which said next instruction should be retrieved is specified within the instruction.

4. (original) A data processing apparatus as claimed in Claim 1, wherein the prediction logic is arranged to detect the presence of an instruction of a second type which when executed can cause said change in instruction flow, and where data identifying the instruction set following said change in instruction flow is specified by the instruction.

5. (original) A data processing apparatus as claimed in Claim 4, wherein said instruction of said second type specifies a register which contains said data identifying the instruction set following said change in instruction flow.

6. (original) A data processing apparatus as claimed in Claim 5, wherein said register also contains an indication of the address within said memory from which a next instruction should be retrieved assuming the change in instruction flow takes place.

7. (original) A data processing apparatus as claimed in Claim 4, wherein said change in the instruction flow occurs only if predetermined conditions are determined to exist at the time that the instruction of said second type is executed.

8. (original) A data processing apparatus as claimed in Claim 1, wherein said prediction logic is a branch prediction logic, and said change in instruction flow results from execution of a branch instruction.

9. (original) A data processing apparatus as claimed in Claim 1, wherein if the prediction logic predicts that execution of said prefetched instruction will cause said change in instruction flow, said prefetched instruction is not passed by the prefetch unit to the processor core for execution.

10. (original) A data processing apparatus as claimed in Claim 9, wherein if said change in instruction flow is dependent on predetermined conditions existing at the time that the prefetched instruction is executed, a condition signal is sent to the processor core for reference by the processor core when executing said next instruction, the processor core being arranged, if said predetermined conditions are determined by the processor core not to exist, to stop execution of said next instruction, and to issue a mispredict signal to the prefetch unit.

11. (original) A data processing apparatus as claimed in Claim 9, wherein said prediction logic is a branch prediction logic, and said prefetched instruction is a branch instruction, said branch instruction being of a type which specifies a subroutine which when completed will cause the instruction flow to return to the instruction sequentially following the branch instruction, the prediction logic being arranged to output a write signal to the processor core to cause the processor core to store an address identifier which can subsequently be used to retrieve said instruction sequentially following the branch instruction.

12. (original) A data processing apparatus as claimed in Claim 1, wherein said prediction logic is contained within said prefetch unit.

13. (original) Prediction logic for a prefetch unit of a data processing apparatus, the data processing apparatus having a processor core for executing instructions from any of a plurality of instruction sets, and said prefetch unit being arranged to prefetch instructions from a memory prior to sending those instructions to the processor core for execution, said prediction logic being arranged to predict which instructions should be prefetched by the prefetch unit, and comprising:

review logic for reviewing a prefetched instruction to predict whether execution of that prefetched instruction will cause a change in instruction flow, and if so to indicate to the prefetch unit an address within said memory from which a next instruction should be retrieved; and

instruction set review logic for predicting whether the prefetched instruction will additionally cause a change in instruction set, and if so to cause an instruction set identification signal to be generated for sending to the processor core to indicate the instruction set to which said next instruction belongs.

14. (original) A method of predicting which instructions should be prefetched by a prefetch unit of a data processing apparatus, the data processing apparatus having a processor core for executing instructions from any of a plurality of instruction sets, and said prefetch unit being arranged to prefetch instructions from a memory prior to sending those instructions to the processor core for execution, the method comprising the steps of:

(a) reviewing a prefetched instruction to predict whether execution of that prefetched instruction will cause a change in instruction flow, and if so indicating to the prefetch unit an address within said memory from which a next instruction should be retrieved; and

(b) predicting whether the prefetched instruction will additionally cause a change in instruction set, and if so causing an instruction set identification signal to be generated for sending to the processor core to indicate the instruction set to which said next instruction belongs.

15. (cancelled).

16. (cancelled).

17. (cancelled).